REMARKS

The Official Action mailed September 27, 2002, has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to January 27, 2003. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on April 4, 2001; June 17, 2002; July 30, 2002; and August 4, 2002. A further *Notice of Related Applications* is submitted herewith and careful review and consideration of this information is requested.

Claims 1-14 were pending in the present application. Applicant notes with appreciation the indication that claims 11-12 are directed to allowable subject matter. Claims 1-6 and 9-12 have been amended herewith and new claims 25-50 have been added to recite additional protection to which Applicant is entitled. Therefore, claims 1-14 and 25-50 are now pending in the present application, of which claims 1, 2, 25, 26, 39, and 40 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Paragraph 2 of the Official Action objects to the drawings asserting that chemical formulas 1-3 attached to the specification are not labeled and do not appear to be discussed in the specification. In response, it is noted that these formulas are discussed on page 43 of the present application and Applicants have amended the specification herewith to insert these formulas into the body of the application as is believed to be customary. No new matter is added and favorable reconsideration is requested in view thereof. Should further amendments be necessary, it is requested the undersigned be contacted so that these formulas can be incorporated in an appropriate manner.

Paragraph 4 of the Official Action rejects Claims 9-12 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. With respect to this rejection, claims 9-12 have been amended herewith and it is respectfully submitted that the informalities noted by the Examiner have been corrected by these amendments. Favorable reconsideration is requested.

Paragraphs 5 and 6 of the Official Action discuss the claim numbering and assert that claims 2, 4, 6, 8, 10, 12 and 14 are objectionable as being substantial duplicates of claims 1, 3, 5, 7, 9, 11 and 13. In response, claims 1 and 2 have been amended herewith such that the claims are now clearly patentably distinct from each other, in which claim 1 is referring to a TFT in a pixel portion and claim 2 is referring a TFT in a driver portion. It is believed that any outstanding objection of the claims is overcome by these amendments. Favorable reconsideration and/or clarification is requested.

Paragraph 7 of the Office Action objects to the title of the application and, in response, the title has been amended to "LIGHT EMITTING DEVICE COMPRISING THIN FILM TRANSISTOR WITH DISTINCT POSITION OF GATE ELECTRODE AND IMPURITY REGIONS." Favorable reconsideration is requested in view thereof.

Paragraph 8 of the Official Action requests Applicant's assistance in correcting any errors that come to applicant's attention and any such errors will be corrected as they come to Applicant's attention.

Paragraph 10 of the Official Action rejects claims 1-10, 13 and 14 as obvious based on the combination of U.S. Patent 5,534,716 to Takemura and Japanese Application No. 7-72675 to Toshiba.

As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

It is respectfully submitted that Takemura and Toshiba, whether taken alone or in combination, fail to disclose or suggest all the claim limitations such that a *prima facie* case of obviousness cannot be maintained. The Examiner is requested to review the attached Exhibit A, submitted herewith in connection with the following discussions highlighting what are believed to be patentably distinguishing features between the present invention and the combination of Takemura and Toshiba.

In Fig. 4E of Takemura, three TFTs including a p-type TFT in a circuit region (left), an n-type TFT in a circuit region (center) and an n-type TFT in a pixel region (right) are shown (see column 6 lines 48-50, and column 7 lines 52-54 and 65-67). Reference number 117 indicates impurity regions of a p-type TFT (column 7 lines 65-67), not a channel forming region of an n-type TFT as asserted in the Official Action. Also, while reference number 118 indicates an n-type impurity region adjacent to the channel forming region, reference number 119 indicates an n-type impurity region in another TFT (column 6 lines 48-50). Since the claimed invention recites a single TFT, it is respectfully submitted that it is unreasonable to interpret Takemura in this fashion and that one of skill in the art would not have been motivated to modify the combination of Takemura and Toshiba in this way. In addition, reference number 120 indicates an interlayer insulating film (column 8 lines 3-5) and reference numbers 122-126 indicate wiring electrodes (column 8 line 10), not a gate insulating layer nor gate electrodes respectively as asserted in the Official Action. Favorable reconsideration is requested in view thereof.

New claims 25-50 are added herewith. New independent claims 25 and 26 further recite a coloring layer that is already recited in claims 11 and 12. Independent claims 39 and 40 recite the features of a TFT as shown in Fig. 1D, but include different expressions from claims 1 and 2. These claims are believed to be allowable for the same reasons as discussed above and favorable consideration of these claims is requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

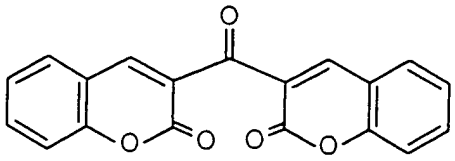
Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

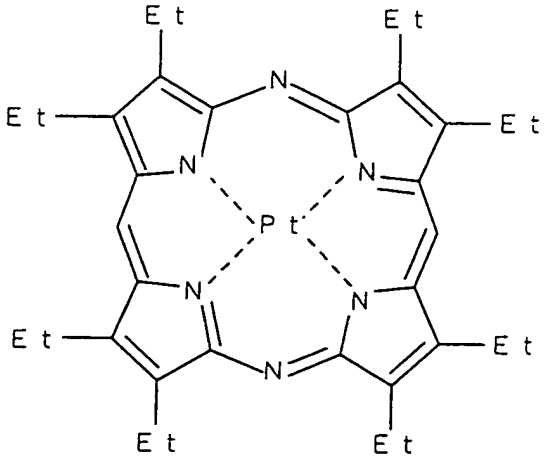
Please amend page 43, to replace "(Chemical formula 1)" with the following formula attached to the application as filed:

[(Chemical formula 1)]



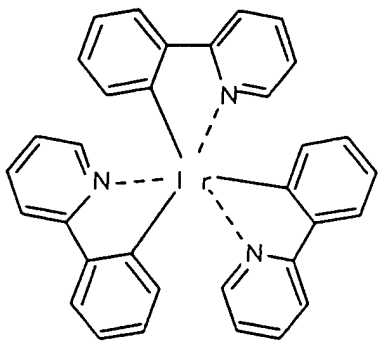
Please amend page 43, to replace "(Chemical formula 2)" with the following formula attached to the application as filed:

[(Chemical formula 2)]



Please amend page 43, to replace "(Chemical formula 3)" with the following formula attached to the application as filed:

[(Chemical formula 3)]



IN THE TITLE:

Please amend the title of the above-identified patent application to:

LIGHT EMITTING DEVICE [AND MANFACTURING METHOD THEREOF] COMPRISING THIN FILM TRANSISTOR WITH DISTINCT POSITION OF GATE ELECTRODE AND IMPURITY REGIONS

IN THE CLAIMS:

Please amend claims 1-6 and 9-12 as follows:

1. (Amended) A light emitting device comprising [an n-channel TFT and a light emitting element in each of pixels, the n-channel TFT comprising]:

a pixel portion having an n-channel TFT and a light emitting element over a substrate,

wherein the n-channel TFT comprises:

an active layer including:

a channel forming region;

an n-type impurity region (c) adjacent to the channel forming region;

an n-type impurity region (b) adjacent to the n-type impurity region (c); and

an n-type impurity region (a) adjacent to the n-type impurity region (b);

a gate insulating layer provided over the active layer; and

a gate electrode provided over the gate insulating layer, the gate electrode including:

a first [gate electrode] conductive film provided over the gate insulating layer; and

a second [gate electrode] conductive film provided over the first [gate] conductive film,

wherein the first [gate electrode] conductive film overlaps the channel forming region and the n-type impurity region (c) with the gate insulating layer interposed therebetween, and

wherein the second [gate electrode] conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed therebetween.

2. (Amended) A light emitting device comprising [a driver circuit comprising a n-channel TFT, and pixel portion comprising a light emitting element, the n-channel TFT comprising]:

a driver circuit having an n-channel TFT over a substrate; and

a pixel portion having a light emitting element over the substrate,

wherein the n-channel TFT comprises:

an active layer including:

a channel forming region;

an n-type impurity region (c) adjacent to the channel forming region;

an n-type impurity region (b) adjacent to the n-type impurity region (c); and

an n-type impurity region (a) adjacent to the n-type impurity region (b);

a gate insulating layer provided over the active layer; and

a gate electrode provided over the gate insulating layer, the gate electrode including:

a first [gate electrode] conductive film provided over the gate insulating layer; and

a second [gate electrode] conductive film provided over the first [gate] conductive film,

wherein the first [gate electrode] conductive film overlaps the channel forming region and the n-type impurity region (c) with the gate insulating layer interposed therebetween, and

wherein the second [gate electrode] conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed therebetween.

3. (Amended) The light emitting device as claimed in claim 1, wherein the first [gate electrode] conductive film comprises one of tantalum nitride and titanium nitride, and the second [gate electrode] conductive film comprises tungsten.

4. (Amended) The light emitting device as claimed in claim 2, wherein the first [gate electrode] conductive film comprises one of tantalum nitride and titanium nitride, and the second [gate electrode] conductive film comprises tungsten.

5. (Amended) The light emitting device as claimed in claim 1, wherein the first [gate electrode] conductive film comprises tungsten, and the second [gate electrode] conductive film comprises aluminum.

6. (Amended) The light emitting device as claimed in claim 2, wherein the first [gate electrode] conductive film comprises tungsten, and the second [gate electrode] conductive film comprises aluminum.

9. (Amended) The light emitting device as claimed in claim 1, wherein the gate electrode is covered by an insulating film [in which] comprising a resin film and at least one of a silicon nitride film and a silicon oxynitride [films are laminated] film.

10. (Amended) The light emitting device as claimed in claim 2, wherein the gate electrode is covered by an insulating film [in which] comprising a resin film and at least one of a silicon nitride film and a silicon oxynitride [films are laminated] film.

11. (Amended) The light emitting device as claimed in claim 9, wherein a coloring layer is provided [on the one of] between the resin film and the silicon nitride film [and] or between the resin film and the silicon oxynitride film [, and the resin film is provided so as to cover the coloring layer].

12. (Amended) The light emitting device as claimed in claim 10, wherein a coloring layer is provided [on the one of] between the resin film and the silicon nitride film [and] or between the resin film and the silicon oxynitride film [, and the resin film is provided so as to cover the coloring layer].

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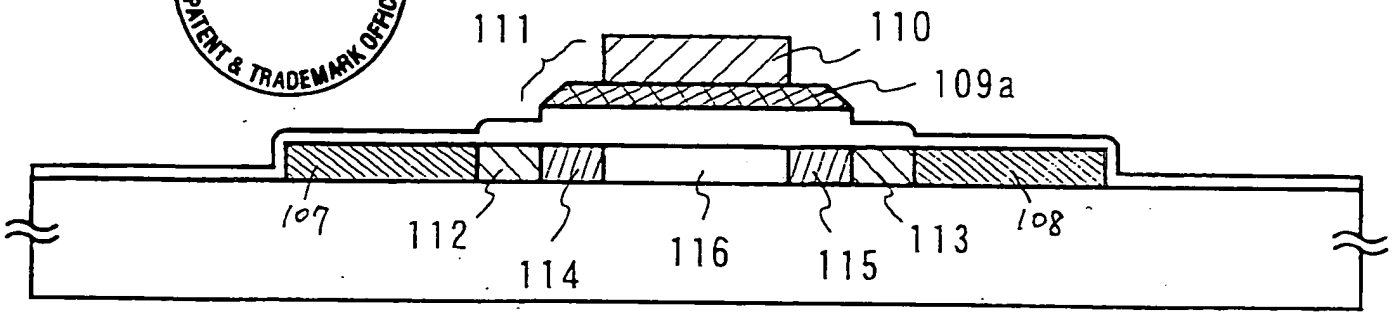
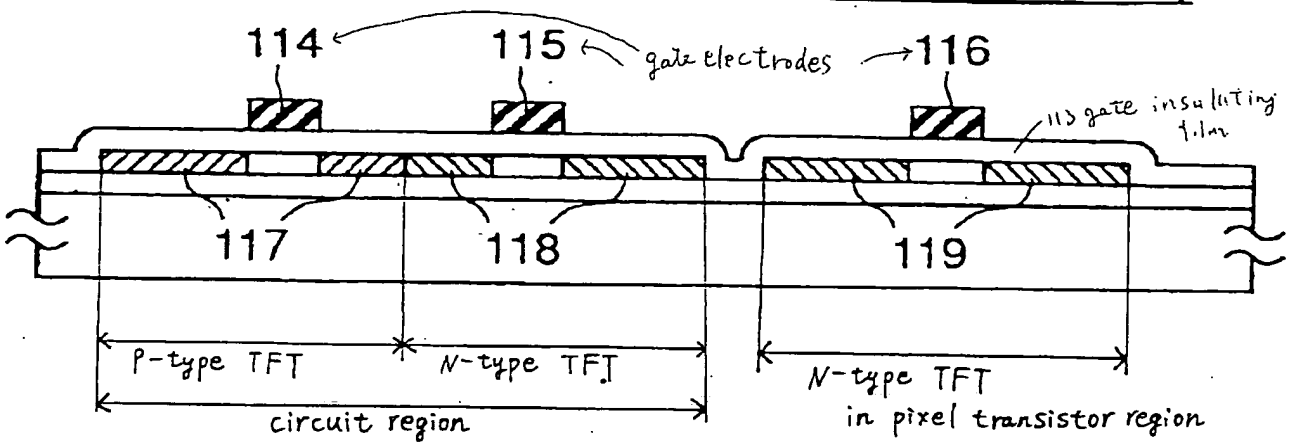
EXHIBIT A



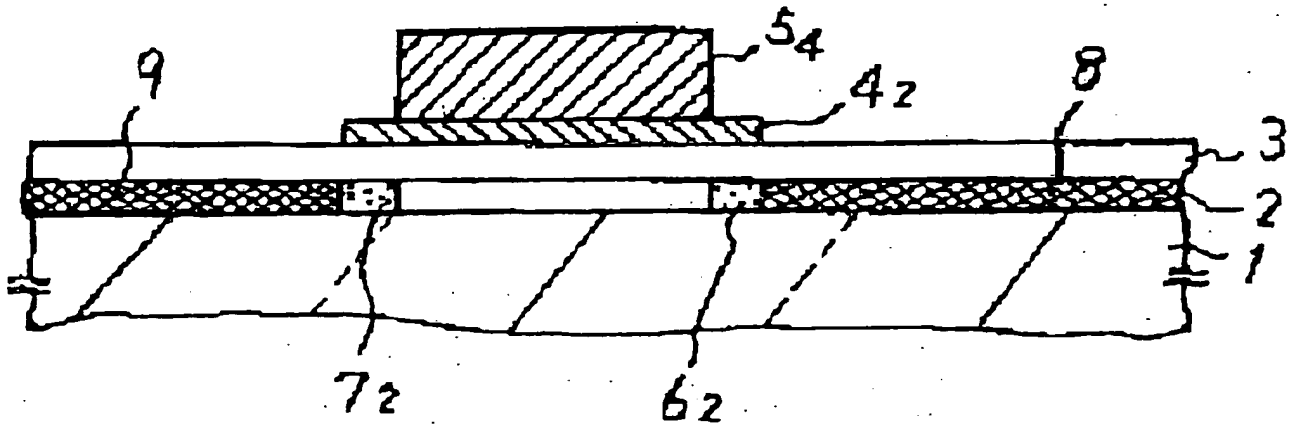
107, 108 - n-type impurity region (a)
112, 113 - n-type impurity region (b)
114, 115 - n-type impurity region (c)

Fig. 1D of the present application



118, 119 - n-type impurity region (a)

Fig. 4E of Takemura (USP 5,534,716)



6_2, 7_2 - n-type impurity region (c)
8, 9 - n-type impurity region (a)

Fig. 2(b) of Toshiba (JP application No. 8-274336)